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STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MN

Office Action Summary	Application No.	Applicant(s)
	10/016,972	ALLEN, ALI
	Examiner	**Art Unit**
	Mardochee Chery	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

42 02-04-08 4)☒ Claim(s) 1-30 ~~1-9 and 27-30~~ is/are pending in the application.

4a) Of the above claim(s) 10-26 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 27-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is a reply to applicants' communication filed on November 14, 2007 in response to PTO Office Action mailed on August 22, 2007. Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-30 remain pending with claims 10-26 withdrawn.

Response to Arguments

3. Applicant's arguments filed November 14, 2007 have been fully considered but they are not persuasive.

a. Applicant's representative argues on page 3, paragraph 2, page 5, paragraph 3, page 6, paragraph 3, page 8, paragraphs 1 and 4, of the remarks that "rather than transferring the requested data from the mass storage device to the host system, Napolitano discloses the predictive retrieval of unrequested data into host memory 330".

Examiner respectfully disagrees. Independent claim 1 recites inter alias "requests a transfer of the requested data that resides in the mass storage device directly to the host system".

In the same manner, Napolitano teaches "DMA engine 356 transfers the information obtained from disks (mass storage) into host

memory 330; col. 10, lines 19-35; DMA 356 transfers the requested data directly into host memory 330; col. 10, lines 62-65".

b. Applicant's representative further asserts on page 4, paragraph 1, page 6, paragraph 4, of the remarks that "Napolitano teaches away from the claim limitation of transferring requested data directly to the host system".

However, such appears to be mere allegations because Napolitano's teaching of "the use of the host CPU 312 to perform transactions can negatively impact data processing performance" simply does not constitute a teaching away of "transferring requested data directly to the host system". It is worth noting that "performing transactions using the host CPU" does not mean "requested data cannot directly be transferred to the host system".

c. In view of the foregoing the rejection of claims 1-9, and 27-30 is maintained as shown in the rejection of the claims below.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lum (5,696,931) over Hicken (6,092,149) and further in view of Napolitano (6,301,605).

As per claim 1, Lum discloses a mass storage system comprising:
a mass storage device (Fig. 1; storage device 104); a cache memory coupled to the mass storage device; the cache memory being organized in data blocks and having a first data block (Fig. 1, disk cache 118, where it is understood that a cache is composed of multiple data blocks); a microprocessor coupled to the mass storage device and the cache memory (Fig. 1, microprocessor 114); and a controller coupled to the microprocessor and the cache memory (Fig. 1; controller 106), wherein the controller: receives a data request from a host system (column 4, lines 4041); calculates new cache counter and pointer values when the first requested data block is not contained within the first block of the cache (column 7, lines 15-62); initiates an auto-transfer of the requested data that resides in the cache to the host system (column 4, lines 40-46); and requests a transfer of the requested data that resides in the mass storage device to the host system (column 9, lines 44-55).

However, Lum might not explicitly teach calculate new cache counter and pointer values when the first requested data block is not contained within the first block of the cache as claimed.

Hicken discloses calculate new cache counter and pointer values when the first requested data block is not contained within the first block of the cache [col. 2, ll 54-65] to process buffered data and commands to and from a host computer in the event of a full cache hit and a partial cache hit (col. 1, ll 23-25; col. 2, ll 55-60).

Since the technology for implementing a disk controller which calculates new cache counter and pointer values when the first requested data block is not contained within the first block of the cache was well known as evidenced by Hicken, an artisan would have been motivated to implement this feature in the system of Lum in order to process buffered data and commands to and from a host computer in the event of a full cache hit and a partial cache hit. Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by Applicant to modify the system of Lum to include calculating new cache counter and pointer values when the first requested data block is not contained within the first block of the cache because this would have helped with processing buffered data and commands to and from a host computer in the event of a full cache hit and a partial cache hit (col. 1, ll 23-25; col. 2, ll 55-60) as taught by Hicken.

However Lum and Hickem might not explicitly teach requesting a transfer of the requested data that resides in the mass storage device directly to the host system.

Napolitano discloses requesting a transfer of the requested data that resides in the mass storage device directly to the host system [col. 10, ll 32-35] so that the data is available at the host if and when requested (col. 10, ll 34-45).

Since the technology for implementing a storage system with teach requesting a transfer of the requested data that resides in the mass storage device directly to the host system was well known as evidenced by Napolitano, an artisan would have been motivated to implement this feature in the system of Lum and Hicken so that the data is available at the host if and when requested. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the system of Lum and Hickem to include requesting a transfer of the requested data that resides in the mass storage device directly to the host system since this would have made the data available at the host if and when requested (col. 10, ll 34-35) as taught by Napolitano.

As per claim 2, Lum discloses a controller register including:
a counter register containing a value for the number of blocks of data in the cache memory (column 5, lines 65-67), a start address register identifying the first block of data in the cache memory (column 6, lines 14-18); and a pointer register containing a pointer to the first block of data in the cache memory (column 8, lines 4-16).

As per claim 3, Lum discloses the microprocessor transfers the requested data that resides in the mass storage device to the host system by way of the cache memory (column 9, lines 44-55).

As per claim 4, Lum discloses the microprocessor controls the transfer of requested data that resides in the mass storage device and the controller controls the transfer of requested data that resides in the cache (column 4, lines 41-47; column 9, lines 44-47).

As per claim 5, Lum discloses the controller includes a general or special purpose processor executing program instructions (Fig. 1, microprocessor 114).

As per claim 6, Lum discloses the transfer of requested data that resides in the mass storage device occurs substantially simultaneously with the transfer of data that resides in the cache (column 9, lines 1-55; column 10, lines 36-38).

6. Claims 8, 27-28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lum (5,696,931) over Simionescu (6,141,728) and further in view of Napolitano (6,301,605).

As per claim 8, Lum discloses a method of retrieving data from a mass storage system comprising: receiving a data request from a host system, the data request including a block address for a first block of the requested data and a number of blocks in the request (column 4, lines 40-41; Fig. 1, disk cache 118, where it is understood that a cache is composed of multiple data blocks; column 5, lines 65-67); if none of the requested data is in a cache memory, initiating a transfer of the requested data from a mass storage device (column 9, lines 44-47); if a portion of the requested data is in the

cache memory and a portion of the requested data is in the mass storage device, transferring the portion of the requested data from the cache memory to the host system substantially concurrently with transferring the portion of the requested data from the mass storage devices to the host system (column 9, lines 1-55; column 10, lines 36-38); if all the requested data is in the cache memory, transferring the requested data from the cache memory to the host system (column 4, lines 41-47); wherein the steps of transferring the requested data from the cache memory system include calculating a starting location in the cache memory for the transfer, based upon the block address and the number of blocks in the request received from the host system (column 5, line 62 - column 6, line 18).

However, Lum might not explicitly teach transferring a portion of the requested data from the cache memory to the host system substantially concurrently with transferring a portion of the requested data from the mass storage devices to the host as claimed.

Simionescu discloses transferring a portion of the requested data from the cache memory to the host system substantially concurrently with transferring a portion of the requested data from the mass storage devices to the host [col. 21, ll 20-26] to quickly and efficiently buffer multiple data transfers into the cache buffer (col. 2, ll 5-10).

Since the technology for implementing a disk controller with transferring a portion of the requested data from the cache memory to the host system substantially concurrently with transferring a portion of the requested data from the mass storage

devices to the host was well known as evidenced by Simionescu, an artisan would have been motivated to implement this feature in the system of Lum in order to quickly and efficiently buffer multiple data transfers into the cache buffer. Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by Applicant, to modify the system of Lum to include transferring a portion of the requested data from the cache memory to the host system substantially concurrently with transferring a portion of the requested data from the mass storage devices to the host because this would have quickly and efficiently buffered multiple data transfers into the cache buffer (col. 2, ll 5-10) as taught by Simionescu.

However Lum and Simionescu might not explicitly teach requesting a transfer of the requested data that resides in the mass storage device directly to the host system.

Napolitano discloses requesting a transfer of the requested data that resides in the mass storage device directly to the host system [col. 10, ll 32-35] so that the data is available at the host if and when requested (col. 10, ll 34-45).

Since the technology for implementing a storage system with teach requesting a transfer of the requested data that resides in the mass storage device directly to the host system was well known as evidenced by Napolitano, an artisan would have been motivated to implement this feature in the system of Lum and Simionescu so that the data is available at the host if and when requested. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the system of Lum and Simionescu to include requesting a transfer of the requested data that resides in the mass storage device directly to the host system since this would have

made the data available at the host if and when requested (col. 10, ll 34-35) as taught by Napolitano.

As per claim 27, the rationale in the rejection of claim 8 is herein incorporated. Lum further discloses a disk memory system, comprising:

a disk-device for storing data-blocks on disk-storage-media (Fig. 1; storage device 104, where it is understood that disk tracks or segments store data blocks); a cache for storing data-blocks (Fig. 1, disk cache 118, where it is understood that a cache is composed of multiple data blocks); a disk-controller (Fig. 1; controller 106); registers within said disk-controller containing a cache-start-address of a first data-block in said cache (column 6, lines 14-18), and a cache-block-length that defines a total number of data-blocks stored in said cache (column 5, lines 65-67); said disk-controller receiving a data-request that contains a request-start-address of a first data-block in said data-request, and a request-block-length that defines a total number of data-blocks in said data-request (column 4, lines 40-41); a microprocessor operationally interconnecting said disk-device, said cache, and said disk-controller (Fig. 1, microprocessor 114); logic means in said disk-controller responsive to said cache-start-address as compared to said request-start-address, and to said cache-block-length-as compared to said request-block-length (column 7, lines 15-62; column 5, line 62 - column 6, line 18); said logic means being operable to determine when no data-blocks corresponding to said data-request reside in said cache, and operating in response to such a determination to cause said microprocessor to fetch said data-blocks corresponding to

said data-request from said disk-device (column 9, lines 44-47); said logic means being operable to determine when all of the data-blocks corresponding to said data-request reside in said cache, and operating in response to such a determination to cause said disk-controller to auto-transfer all of said data-blocks corresponding to said data-request from said cache without requiring operation of said microprocessor (column 4, lines 40-46); and said logic means being operable to determine when a cache-hit-portion of data-blocks corresponding to said data-request reside in said cache and a cache-miss-portion of said data-blocks corresponding to said data-request do not reside in said cache, and operating in response to such a determination to concurrently cause said disk-controller to auto-transfer said cache-hit-portion of said data-blocks corresponding to said data-request from said cache, and to cause said microprocessor to fetch data-blocks corresponding to said cache-miss-portion of said data-request from said disk-device (column 9, lines 1-55; column 10, lines 36-38).

As per claim 28, the rationale in the rejection of claim 8 is herein incorporated. Lum further discloses a disk memory system, comprising:

a relatively slow disk-device for storing data-blocks on disk-storage-media (Fig. 1; storage device 104, where it is understood that disk tracks or segments store data blocks); a relatively fast cache for storing data-blocks (Fig. 1, disk cache 118, where it is understood that a cache is composed of multiple data blocks); a disk-controller (Fig. 1; controller 106), and a microprocessor (Fig. 1, microprocessor 114); registers within said disk-controller containing a cache-start-address of a first data-block in said cache

(column 6, lines 14-18), and a cache-block-length that defines a total number of data-blocks stored in said cache (column 5, lines 65-67); said disk-controller receiving as input a data-request from said host-system; said data request containing a request-start-address of a first data-block in said data-request, and a request-block-length that defines a total number of data-blocks in said data-request (column 4, lines 40-41); a logic circuit in said disk-controller responsive to said cache-start address as compared to said request-start-address, and to said cache-block-length as compared to said request-block-length (column 9, lines 44-47); said logic circuit being operable to determine a cache-miss when no data-blocks corresponding to said data-request reside in said cache, and operating in response to a cache-miss to cause said microprocessor to fetch said data-blocks corresponding to said data-request from said disk-device (column 9, lines 44-47); said logic circuit being operable to determine a total-cache-hit when all of the data-blocks corresponding to said data-request reside in said cache, and operating in response to a total-cache-hit to cause said disk-controller to auto-transfer all of said data-blocks corresponding to said data-request from said cache without requiring operation of said microprocessor (column 4, lines 40-46); and said logic circuit being operable to determine a partial-cache-hit when a first-portion of data-blocks corresponding to said data-request reside in said cache and a second-portion of said data-blocks corresponding to said data-request do not reside in said cache, and operating in response to a partial-cache-hit to concurrently cause said disk-controller to auto-transfer said first-portion of said data-blocks corresponding to said data-request from said cache, and to cause said microprocessor to fetch data-blocks corresponding

to said second-portion of said data-request from said disk-device (column 9, lines 1-55; column 10, lines 36-38).

As per claim 30, Simionescu discloses the logic means include a processor executing programmed instructions [Fig. 1].

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lum et al (US 5,696,931) in view Hicken (6,092,149), Napolitano (6,301,605), and of well-known practices in the art.

Regarding claim 7, Lum discloses the claimed invention as per the rejection of claim 1 supra. Lum does not explicitly disclose the mass storage system and the host system are integrated into a single unit as required in the claim. However, to make integral is generally not given patentable weight.

Furthermore, integrating memory and logic on a single device is a common and well-known practice in the art, to reduce pin count, power and area, and to increase the data transfer rate between elements. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention by applicant to integrate the mass storage and the host in the system of Lum to reduce pin count, power and area, and to increase the data transfer rate between elements based on conventional practices.

8. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lum et al (US 5,696,931) in view Simionescu (6,141,728), Napolitano (6,301,605) and of well-known practices in the art.

Regarding claim 29, Lum discloses the claimed invention as per the rejection of claim 28 supra. Lum does not explicitly disclose the mass storage system and the host system are integrated into a single unit as required in the claim. However, to make integral is generally not given patentable weight.

Furthermore, integrating memory and logic on a single device is a common and well-known practice in the art, to reduce pin count, power and area, and to increase the data transfer rate between elements. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention by applicant to integrate the mass storage and the host in the system of Lum to reduce pin count, power and area, and to increase the data transfer rate between elements based on conventional practices.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lum et al (US 5,696,931) in view of Simionescu (6,141,728), Napolitano (6,301,605) and Taroda et al (US Pub 200110014929) A1).

As per claim 9, Lum, Simionescu, and Napolitano disclose the claimed invention as per the rejection of claim 8 supra. Lum, Simionescu, and Napolitano do not

explicitly disclose the data request has a first logical address protocol and the cache memory has a second logical address protocol and including the step of translating between the first and second address protocols as required in the claim.

Taroda discloses a disk control device having a block format different from the host wherein the first and second formats can be converted (Paragraphs 12-16) to realize access compatible with the two different formats.

Thus, it would have been obvious to one of ordinary skill at the time of the invention by applicant, to modify the system of Lum and Simionescu to include converting formats between the host and the disk controller in the manner taught by Taroda, because it was well known to realize access compatible with the two different formats (Paragraph 14) as taught by Taroda.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

12. When responding to the Office action, Applicant is advised to clearly point out where support, with reference to page, line numbers, and figures, is found for any amendment made to the claims.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

February 4, 2008

Mardochee Chery
Examiner
AU: 2188

HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER
02/04/08